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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,922	08/27/2003	Kiran V. Chatty	BUR920030045US1	1921

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,922	CHATTY ET AL.	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *1* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/27/03, 9/8/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of claims 2-19 in the reply filed on 10/12/2004 is acknowledged. The traversal is on the ground(s) that examination of the entire application can be made without serious burden on the examiner, because the claims appear to be part of the same technology (semiconductor devices). This is not found persuasive because although both inventions relate to semiconductor devices, examination of two distinct inventions creates serious burden on the examiner.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

Claims 1-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of "having no n-diffusions connected directly to it" and "no n-diffusions directly connected", as recited in claims 2 and 11, are unclear as to which elements the n-diffusions are connected or not connected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-9 and 11-18, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Schroder (6,215,135) in view of White et al. (5,589,423).

Regarding claims 2 and 11, Schroder teaches in figure 1 and related text a latch-up robust ESD integrated circuit comprising: one or more I/0 cells each having one or more I/0 pads BP with no n-diffusions directly connected and wherein each of said one or more I/0 pads is coupled to an associated and distinct one or more silicide blocked p-type field effect transistors having a source, drain, gate, and gate oxide, said transistor further having a snapback voltage that is less than the breakdown voltage of said gate oxide.

Regarding the claimed limitations of a transistor having a snapback voltage that is less than the breakdown voltage of said gate oxide, these features are inherent in Schroder's device, because Schroder's structure is identical to the claimed structure.

Regarding the claimed limitation of a silicide blocked p-type field effect transistor, Schroder teaches an ESD device which does not comprise silicide. Therefore, forming the device using a silicide blocked p-type field effect transistor is a

process limitation which would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Therefore, Schroder's structure is at least obvious over the claimed structure.

In the alternative, White et al. forms a silicide blocked p-type field effect transistor by using a silicide blocked layer (see abstract).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a silicide blocked p-type field effect transistor in Schroder's device in order to prevent silicidation of protective devices.

Regarding claims 3 and 12, Schroder teaches said source is coupled to a voltage and said gate is coupled to said source and said drain is coupled said 1/0 pad.

Regarding claims 4-5 and 13-14, Schroder teaches in figure 2 a body terminal coupled to the source of the transistor.

Regarding claims 6 and 15, 6, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a snapback voltage of at most 5 volts in Schroder's device in order to use the device in an application which requires a snapback voltage of at most 5 volts.

Regarding claims 7-9 and 16-18, Schroder teaches in figure 2 a resistor coupled to said transistor and coupled said I/0 pad. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a p type resistor in Schroder's device in order to simplify the processing steps of making the device by forming a p type diffusion resistor in the substrate.

Claims 10 and 19, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Schroder and White et al., as applied to claims 2, 7, 11 and 16 above, and further in view of Applicant Admitted Prior Art (AAPA).

Schroder and White et al. teach substantially the entire claimed structure, as applied to claims 2, 7, 11 and 16 above, except forming the resistor between said transistor and said I/0 pad. AAPA teaches in figure 1 forming a resistor between the protection device and the I/0 pad. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form prior art's

resistor between said transistor and said I/0 pad, so that a first voltage appearing at said I/0 pad is of a different magnitude than a second voltage appearing at said transistor, said first and second voltages differing by a value proportional to the resistance of said p-type resistor, in order to improve the protection capability of the device.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.
Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
11/17/04

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800